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EXAMINER
DARE, RYAN A

ART UNIT	PAPER NUMBER
2186	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

	Application No.	Applicant(s)
Office Action Summary	10/828,992	BOMBAL, JEROME
	Examiner	Art Unit
	RYAN DARE	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _22 September 2008_.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-24_ is/are pending in the application.
　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-24_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
　　a)☐ All   b)☐ Some * c)☐ None of:
　　　　1.☐ Certified copies of the priority documents have been received.
　　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.
　　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)
1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
obviousness or nonobviousness.

3.   Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Jaggar et al., US Patent 6,343,358, in view of Campbell et al., US Patent 6,848,042 .

4.   With respect to claim 1, Jaggar teaches an electronic device, comprising:

a memory structure comprising an integer M of memory word slots, wherein each

memory word slot is operable to store an integer N of bits, in col. 5, line 61 through col.

6, line 2;

a scan storage circuit, operable to receive a scan word having a number of bits

less than MxN, in col. 4, lines 29-37

control circuitry for causing successive scan words to be written into the scan

storage circuit, for causing successive scan words to be written from the scan storage

circuit into the memory word slots of the memory structure, and for causing successive scan words to be read from the memory word slots of the memory structure into the scan storage circuit, in col.4, line 66 through col. 5, line 6.

Jaggar fails to teach the specifics of the memory structure and that it is a FIFO.

Campbell teaches a memory structure comprising an integer M of memory word slots wherein the integer M is greater than one, wherein each memory word slot is operable to store an integer N of bits and wherein the integer M of memory word slots are arranged in a first-in first-out configuration, in col. 3, lines 31—7. Campbell further teaches successive words to be written into a storage circuit, for causing success words to be written from the storage circuit into all of the memory word slots of the memory structure, and for causing successive words to be read from all of the memory words slots into the storage circuit, in col. 6, lines 5-13. Therefore the combination of Jaggar and Campbell teach all limitations of the present claim.

5.   It would have been obvious to one of ordinary skill in the art, having the teachings of Jaggar and Campbell before him at the time the invention was made, to modify the electronic memory device of Jaggar with the electronic memory device of Campbell in order to be able to input and output data from a memory at high speed, as taught by Campbell in col. 1, line 66 through col. 2, line 9.

6.   With respect to claim 2, Jaggar teaches the electronic device of claim 1 wherein the scan storage circuit is operable to receive a scan word consisting of N bits, in col. 4, lines 29-37 and col. 4, line 66 through col. 5, line 6.

7.   With respect to claim 3, Jaggar teaches the electronic device of claim 2 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit, in col. 4, line 66 through col. 5, line 6.

8.   With respect to claim 4, Jaggar teaches the electronic device of claim 3 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as corresponding successive scan word is written into the scan storage circuit, in col. 4, line 66 through col. 5, line 6.

9.   With respect to claim 5, Jaggar teaches the electronic device of claim 4 wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in col. 4, line 66 through col. 5, line 6.

10.   With respect to claim 6, Jaggar teaches the electronic device of claim 5:

        wherein the successive scan words to be written into the scan storage circuit comprise a test sequence, in col. 1, lines 30-36; and

        further comprising circuitry for comparing the successive scan words to be read from the memory structure to the test sequence, in col. 4, line 66 through col. 5, line 6.

11.   With respect to claim 7, Jaggar teaches the electronic device of claim 6: wherein each memory word slot is operable to store the integer N of bits in a corresponding set

of N memory cells; and wherein each set of N memory cells comprises N latches, in col. 4, lines 29-37 and col. 4, line 66 through col. 5, line 6;

12.   With respect to claim 8, Jaggar teaches the electronic device of claim 7 wherein each of the N latches comprises: a first inverter having an input providing an input to the latch and an output providing an output of the latch; and a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch, because this is the definition of a latch. It is inherent that the Jaggar reference teaches such a latch.

13.   With respect to claim 9, Jaggar teaches the electronic device of claim 7 wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells, in col. 5, lines 7-57; and

        wherein each set of N memory cells is operable to store incoming data without responding to a clock transition, in col. 5, lines 7-57, where in debug mode, it operates without the main clock signal.

14.   With respect to claim 10, Jaggar teaches the electronic device of claim 7 wherein the width N is selected from a group consisting of 128, 64, 32, 16, 8, and 4, in col. 4, line 38.

15.   With respect to claims 11-13, Applicant claims the same electronic device as claims 2-5 but dependent on claim 1, and are therefore rejected using similar logic.

16.   With respect to claim 14, Applicant claims the same electronic device as claims 4-5 and is therefore rejected using similar logic.

17.   With respect to claims 15-16 Applicant claims the same electronic device as claims 7-8 and is therefore rejected using similar logic.

18.   With respect to claim 17, Jaggar teaches the electronic device of claim 1 wherein the memory structure, the scan storage circuit, and the control circuitry are all in a single integrated circuit, in col. 4, lines 29-37.

19.   With respect to claims 18-20, Applicant claims a method of operating an electronic device that corresponds the electronic device of claims 1-3 and is therefore rejected using similar logic.

20.   With respect to claim 21, Jaggar teaches the method of claim 19 and further comprising causing each successive scan word to be serially read by shifting bits out from the scan storage circuit during a same time period as causing corresponding successive scan words to be serially written by shifting bits into the scan storage circuit, in col. 4, line 66 through col. 5, line 6.

21.   With respect to claim 22, Applicant claims a method that corresponds to the electronic device of claim 5 and is therefore rejected using similar logic.

22.   Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar and Campbell as applied to claims 1 and 18 above, in view of Freidlin et al., US Patent 5,995,988.

23.   With respect to claim 23, Jaggar and Campbell teach all limitations of the parent claim, but fail to teach a single serial shift storage circuit. Freidlin teaches the electronic device of claim 1 wherein the scan storage circuit comprises a single serial shift storage

circuit consisting of the integer N of bits and for serially causing each successive scan word to be read one bit at a time from the single serial shift storage circuit during a same time period as a corresponding successive scan word is written one bit at a time into the same single serial shift storage circuit, in col. 3, lines 40-48.

24.   It would have been obvious to one of ordinary skill in the art, having the teachings of Jaggar, Campbell and Freidlin before him at the time the invention was made, to modify the electronic memory device of Jaggar and Campbell with the electronic memory device of Freidlin in order to be able to, as taught Freidlin in order to be able to break up the N bits into different sizes, therefore allowing more adaptability and speed in the memory system, as taught by Freidlin in col. 7, lines 33-47.

25.   With respect to claim 23, Jaggar and Campbell teach all limitations of the parent claim, but fail to teach a single serial shift storage circuit. Freidlin teaches the method of claim 18 wherein the scan storage circuit comprises a single serial shift storage circuit consisting of the integer N of bits and for serially causing each successive scan word to be read one bit at a time from the single serial shift storage circuit during a same time period as a corresponding successive scan word is written one bit at a time into the same single serial shift storage circuit, in col. 3, lines 40-48.

26.   It would have been obvious to one of ordinary skill in the art, having the teachings of Jaggar, Campbell and Freidlin before him at the time the invention was made, to modify the electronic memory device of Jaggar and Campbell with the electronic memory device of Freidlin in order to be able to, as taught Freidlin in order to

be able to break up the N bits into different sizes, therefore allowing more adaptability

and speed in the memory system, as taught by Freidlin in col. 7, lines 33-47.

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Response to Arguments

27.   Applicant's arguments with respect to claims 1-24 have been considered but are

moot in view of the new ground(s) of rejection. The Campbell and Freidlin references,

combined with the original Jaggar reference, teach the limitations added in the claim

amendments.

Conclusion

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to RYAN DARE whose telephone number is (571)272-

4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Dare/
December 7, 2008

                                                        /Pierre-Michel Bataille/
                                                        Primary Examiner, Art Unit 2186